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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/316,560	05/24/1999	MARC DURANTON	PHF-99.540V	7958

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	36

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/316,560	DURANTON, MARC	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04 March 2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller (5,027,330).

As per claims 1, 4, and 5, Miller teaches a system incorporating an asynchronous FIFO circuit. The system includes, with reference to figure 3, an input processor 5 ("first processor") for writing to the FIFO and an output processor 15 ("second processor") for reading from the FIFO. See also column 2, lines 3-9. The memory circuit includes a plurality of FIFO circuits 100, 150. The reset circuit 215 and flag circuit 210 represent the "master controller" of claim 1. FIFO status signals and the reset signal 8 represent "control commands". The system of Mason

also includes a write control circuit 205, write pointer 235, read control circuit 220, and a read pointer 245 (collectively a "control unit", where the pointers are actually counters incremented based on signals from their respective control circuits). These pointers are loaded based on a write enable signal from the input processor and read enable signals received from the output processor. See figure 2 and column 3, lines 37-66.

As per claim 2, as set forth previously, Miller teaches a write pointer and a read pointer, which indicate the addresses to which data is written and read from.

As per claim 3, Miller teaches, with reference to figures 2-3, read port (elements 2 and "output data bus" 11) and write port (element 7 and "input data bus" 6).

As per claim 4, Miller teaches a flag circuit 210 (figure 2), which indicates when the FIFO is empty (E), half-full (HF), and full (F). See column 2, lines 55-60. This circuit tracks the difference in the values between the read and write pointers and outputs the E, HF, or F signals based on the difference. See column 1, lines 19-24. This process is performed in part so that the FIFO rejects any attempt to store data in the memory when full (i.e. preventing the read and write pointers from simultaneously trying to access the same memory location). See column 1, lines 34-44. The "comparator" is represented by the element that determines the difference between the read and write pointers.

Response to Arguments

4. Applicant's arguments filed 04 March 2004 have been fully considered but they are not persuasive.

With respect to claim 4, Applicant argues that Miller does not teach a "comparator". However, Miller teaches a "comparator" performing the limitation set forth in the claim as set forth above.

With respect to claims 1 and 5, Applicant argues that Miller et al. does not teach "using control commands associated with a set of input data and a set of output data". However, the limitation of "using control commands associated with a set of input data and a set of output data" is a very broad limitation. For example, Applicant has not set forth in the claim the exact "association" between the control commands and the input/output data, and therefore even the most minute link between the "control commands" and the "input data" and "output data" would teach the limitation. In a similar manner, the term "control commands" is broad, and the reset signal 8 and empty (E), half-full (HF), and full (F) signals (16, 14, 13) cause (i.e. command) the reset circuit and read and write control circuits to perform various control actions. The actions performed by the reset circuit 215 and flag circuit 210 teach the broad limitation of "using control commands associated with a set of input data and a set of output data".

Conclusion

5. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
April 15, 2004